the error correction done by said error correcting means, based on the syndrome transmitted from said syndrome calculating means; and

a first transfer resuming sub means for, after the completion of the second transfer, making the first transfer sub means resume the first transfer for subsequent code words including the code word which has been subjected to the second transfer, and

said error detecting means comprises:

a first error detecting sub means for, until said syndrome calculating means detects an error-containing code, executing a first error detection where error detection is performed for a code word transmitted from said buffer memory in parallel with the syndrome calculation done by said syndrome calculating means, while storing mid-term results of the error detection in code word units to said storing means;

a second error detecting sub means for, after said syndrome calculating means detects an error-containing code, executing a second error detection where error detection is resumed for code words whose errors have been detected and corrected by said error correcting means, starting at a code word which has previous contents before the occurrence of an error and which is already stored in said storing means; and

a first error detection resuming sub means for, after the completion of the second error detection for the error-corrected code word, making the first error detecting sub means resume the first error detection for subsequent code words.

6. The error correction device of claim 5 further comprising a DMA

control means for controlling DMA transfer to said buffer memory, wherein said system control means comprises:

a DMA transfer instruction sub means for providing said DMA control means with a DMA transfer instruction indicating that data to be corrected should be transferred from said buffer memory to said syndrome calculating means and to said error detecting means at the start of an error correcting process; and

said DMA control means comprises a data transfer control sub means for making a request of said bus control means to perform DMA transfer in accordance with the DMA transfer instruction transmitted by said system control means.

7. An error correction device comprising; a buffer memory for storing at least one ECC block of data having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to error correction; a syndrome calculating means for generating syndrome for data read from said buffer memory; an error correcting means for correcting error-containing data in said buffer memory by detecting an error position from the syndrome generated by said syndrome calculating means and by calculating an error value; an error detecting means for detecting an error in error-corrected

data generated by said error correcting means; a bus control means for controlling data transfer between said buffer memory, said syndrome calculating means, said error correcting means, and said error detecting means; and a system control means for performing various processes for error correction in predetermined procedures a necessary number of times, wherein

said system control means comprises:

a first-time error correction sub means for reading data from said buffer memory in a same direction as calculation for an error detecting code as a first-time error correction; for transferring the read data to said syndrome calculating means and to said error detecting means concurrently until said syndrome calculating means detects an error-containing code; for making said syndrome calculating means execute syndrome calculation and said error detecting means execute error detection in parallel; for making said error correcting means execute error correction when said syndrome calculating means has detected an error-containing code; and for making one of said syndrome calculating means and said error correcting means provide the system control means with information which designates a code word containing the error-containing code;

an even-numbered error correction sub means for reading a code word in a different direction from a preceding odd-numbered error correction; for transferring the code word to said syndrome calculating means and to said error detecting means concurrently until said syndrome calculating means detects an error-containing code; for making said syndrome calculating